RTL8723DS-CG

SINGLE-CHIP 802.11b/g/n 1T1R WLAN and BLUETOOTH 2.1/4.2 with SDIO INTERFACE, and HS-UART MIXED INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.80	2016/3/30	Preliminary release.
0.90	2016/3/30	Fix BT description
0.91	2017/3/23	Modify mark on pin 1， rename pin VBAT_OUT, VBAT_IN, VBAT_EN to VD33D, VD33D, GND
0.92	2017/7/24	Modify SDIO/GSPI/UART interface power on sequence, modify description of pin 41 and pin 28 for GPIO IO power reference

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1. General Description

The Realtek RTL8723DS is a highly integrated 802.11b/g/n 1T1R WLAN and Bluetooth 2.1/4.2 single chip . It combines a WLAN MAC, a 1T1R capable WLAN baseband, BT Protocol Stack (LM, LL, and LE), BT Baseband, modem, and WLAN/BT RF in a single chip. The RTL8723DS provides a complete solution for a high throughput performance integrated wireless LAN, and Bluetooth.

The RTL8723DS WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 1 transmit and 1 receive path and is compatible with the 802.11n specification. Features include one spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide higher data rates of 54Mbps and 150Mbps for 802.11g and 802.11n OFDM respectively.

A built-in enhanced signal detector, adaptive frequency domain equalizer, and a soft-decision Viterbi decoder help to alleviate multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8723DS WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain better performance in the analog portions of the transceiver.

The RTL8723DS WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensate for the extra power required to transmit OFDM. The RTL8723DS provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

The RTL8723DS Bluetooth controller complies with Bluetooth core specification v4.2, and supports dual mode (BR/EDR + Low Energy Controllers). It is compatible with previous versions, including v2.1 + EDR. For BR/EDR, it supports scatternet topology and allows active links in slave mode, and active links in master mode. For Low Energy, it supports multiple states and allows active links in master mode. The links in BR/EDR and LE can be active simultaneously.

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2. Features

General

- QFN48 6 x 6 mm
- 802.11b/g/n 1T1R WLAN, and Bluetooth single chip

Host Interface

- Complies with SDIO 1.1/2.0 for WLAN with clock rate up to 100MHz (SDR50 and DDR50)
- GSPI interface for configurable endian for WLAN
- Complies with HS-UART with configurable baud rate for Bluetooth

WLAN Controller

- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode
- 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g; and 150Mbps in 802.11n
- Switch diversity for DSSS/CCK
- Packet based hardware antenna diversity

- Selectable receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Bluetooth Controller

- Compatible with Bluetooth v2.1+EDR and v4.2 Systems
- Supports Bluetooth 4.0 Low Energy(BLE)
- HS-UART interface for Bluetooth data transmission compliant with H5 specification
- PCM interface for audio data transmission via Bluetooth controller
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link (allows one link for PCM interface and three links for HS-UART)
- Supports piconets in a scatternet
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff/Sniff Sub-rating)
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Power Control/Enhanced Power Control
- Bluetooth Low Energy Support
- Integrated 32K oscillator for power management

Peripheral Interfaces

- General Purpose Input/Output (14 pins)
- Two configurable LED pins

3. Application Diagram

3.1. Integrated Single-Band 11n (1x1) and Bluetooth Controller with Antenna Diversity

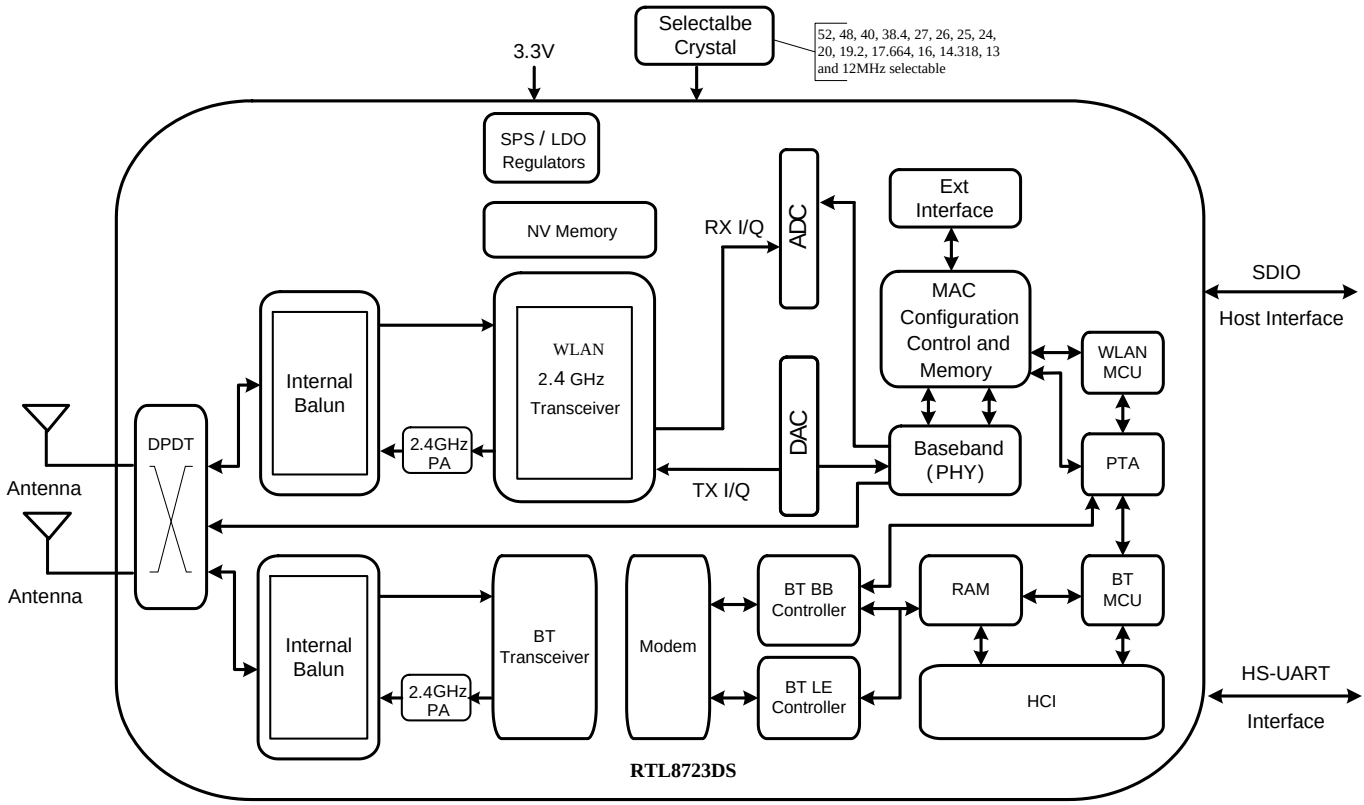


Figure 1. RTL8723DS with antenna diversity

3.2. Integrated Single-Band 11n (1x1) and Bluetooth Controller with WL/BT Shared antenna

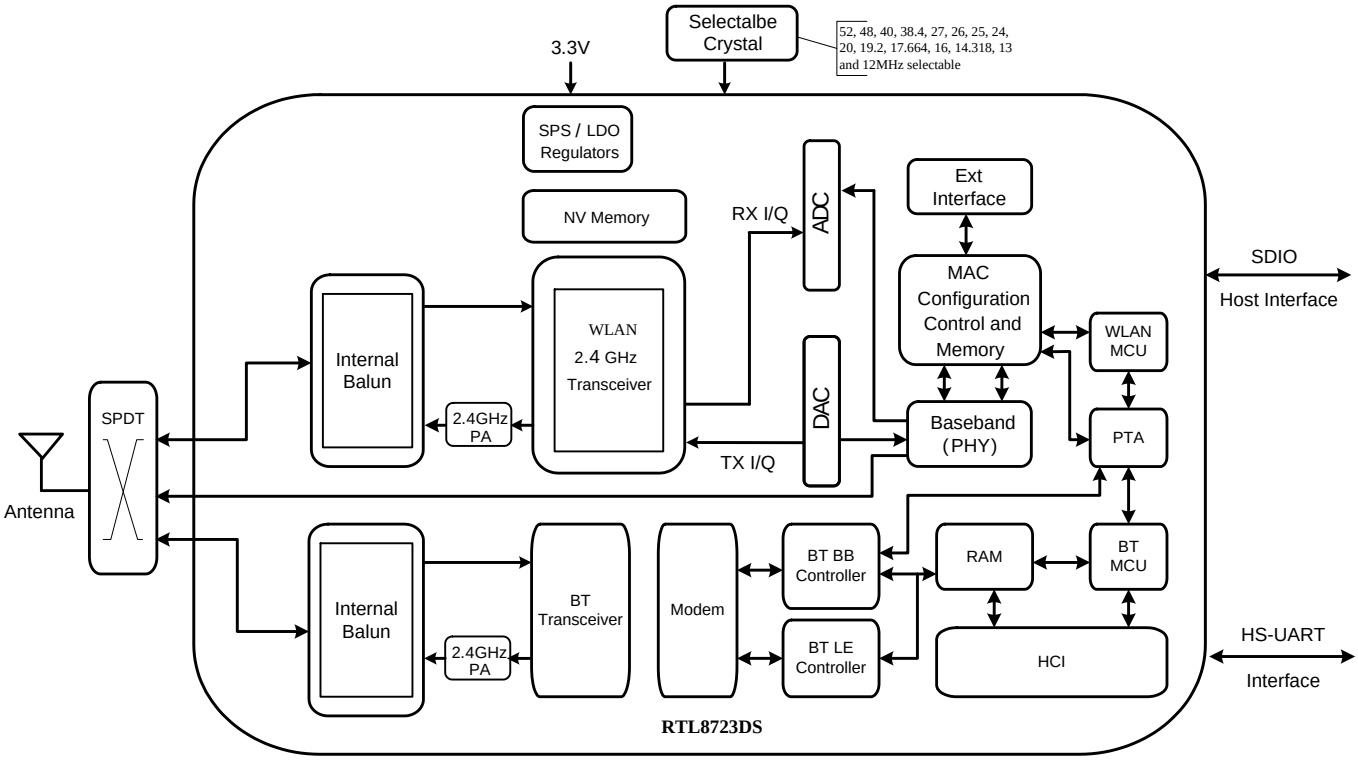


Figure 2. RTL8723DS with shared antenna between WLAN and Bluetooth

4. Pin Assignments

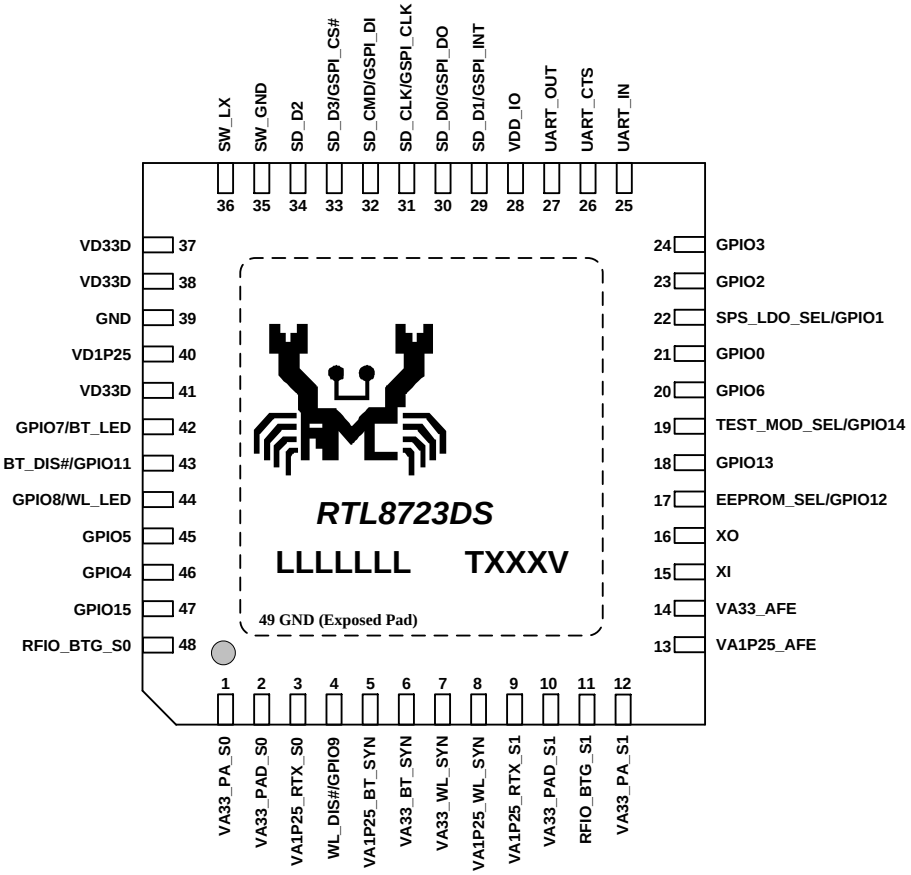


Figure 3. Pin Assignments

5. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 3. The version is shown in the location marked 'V', e.g., Q=Version Q.

6. Pin Descriptions

The following signal type codes are used in the tables:

I: Input O: Output

6.1. Power-On Trap Pins

Table 1. Power On Trap Pins

Symbol	Type	Pin No	Description
TEST_MODE_SEL	I	19	Shared with GPIO14 0: Normal operation mode 1: Enter into test/debug mode
SPS_LDO_SEL	I	22	Shared with GPIO1 0: Internal switching regulator select 1: Internal LDO select
EEPROM_SEL	I	17	Shared with GPIO12 pin 0: Internal NV memory select 1: External EEPROM select

6.2. SDIO Interface

Table 2. SDIO Interface

Symbol	Type	Pin No	Description
SD_CLK	I	31	SDIO Clock Input
SD_CMD	IO	32	SDIO Command Input
SD_D0	IO	30	SDIO Data Line 0
SD_D1	IO	29	SDIO Data Line 1
SD_D2	IO	34	SDIO Data Line 2
SD_D3	IO	33	SDIO Data Line 3

Note: Refer to section 7.4.1, page 15 for SDIO signal level selection.

6.3. GSPI Interface

Table 3. GSPI Interface

Symbol	Type	Pin No	Description
GSPI_CLK	I	31	GSPI Clock Input
GSPI_DI	I	32	GSPI Data Input
GSPI_DO	O	30	GSPI Data Out
GSPI_INT	O	29	GSPI Interrupt
GSPI_CS#	I	33	GSPI Chip Select

Note 1: GSPI and SDIO are shared pins.
Note 2: Refer to section 7.4.1, page 15 for GSPI signal level selection.

6.4. HS-UART Transceiver Interface

Table 4. HS-UART Interface

Symbol	Type	Pin No	Description
UART_OUT	O	27	High-Speed UART Data Out

Symbol	Type	Pin No	Description
UART_CTS	I	26	High-Speed UART CTS
UART_IN	I	25	High-Speed UART Data In

Note: Refer to section 7.5.1, page 19 for UART signal level selection.

6.5. PCM Interface

Table 5. PCM Interface

Symbol	Type	Pin No	Description
PCM_IN	I	21	PCM data Input, shared with GPIO0
PCM_OUT	O	22	PCM data Out, shared with GPIO1
PCM_SYNC	O	23	PCM Synchronization control, shared with GPIO2
PCM_CLK	IO	24	PCM Clock, shared with GPIO3

Note: Refer to section 7.5.1, page 19 for PCM signal level selection.

6.6. RF Interface

Table 6 RF Interface

Symbol	Type	Pin No	Description
RFIO_BTG_S0	IO	48	WLAN/BT RF TX/RX signal port 0
RFIO_BTG_S1	IO	11	WLAN/BT RF TX/RX signal port 1

6.7. LED Interface

Table 7 LED Interface

Symbol	Type	Pin No	Description
BT_LED	O	42	LED Pin (Active Low)
WL_LED	O	44	LED Pin (Active Low)

Note: These IO pins refer to the IO level from pin 41 (VD33D)

6.8. Power Management Handshake Interface

Table 8 Power Management Handshake Interface

Symbol	Type	Pin No	Description
WL_DIS#	I	4	Shared with GPIO9. This pin can externally shut down the RTL8723DS WLAN function when WL_DIS# is pulled low. When this pin is pulled low, SDIO interface will be disabled. This pin can also be configured as the WLAN Radio-off function with host interface remaining connected.
BT_DIS#	I	43	Shared with GPIO11. This pin can externally shut down the RTL8723DS BT function when BT_DIS# is pulled Low. When this pin is pulled low, uart interface will be also disabled. This pin can be also defined as the BT Radio-off function with host interface remaining connected.
DEV_WAKE_HOST_WL	O	20	Shared with GPIO6 This pin is used by WIFI to wake up the host when the remote wake function is enabled. The polarity can be defined by the customer. This Wakeup pin can be configured as wakeup pin by WL when WL function issue the wake signal to the host.
DEV_WAKE_HOST_BT	O	19	Shared with GPIO14 This pin is used by BT functions to wake up the host when the remote wake function is enabled. The polarity can be defined by the customer. This Wakeup pin can be configured as wakeup pin by BT when BT function issue the wake signal to the host.
HOST_WAKE_DEV	I	18	Shared with GPIO13 This pin can be configured as the host wakes up the WLAN or Bluetooth controller or both of them in Remote Wakeup Mode.
CLKREQ	O	47	Shared with GPIO15. When RTL8723D XTAL clock is fed from host chipset, it will assert CLKREQ to request XTAL clock. Otherwise, RTL8723DS will de-assert CLKREQ to indicate host chipset that there is no need to output the XTAL clock to RTL8723DS. This signal is used for power saving control with host chipset.

6.9. Clock and Other Pins

Table 9. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	15	OSC Input Input of Crystal Clock Reference, the frequency of Crystal can be: 40MHz, 25MHz, 13MHz, 19.2MHz, 20MHz, 26MHz, 38.4MHz, 17.664MHz, 16MHz, 14.318MHz, 12MHz, 52MHz, 48MHz, 27MHz, 24MHz
XO	O	16	Output of 26MHz/40MHz Crystal Clock Reference
SUS_CLK/ SPS_LDO_SEL	I	22	Shared with GPIO1. External 32K or RTC clock input.
GPIO0	IO	21	General Purpose Input/Output Pin
GPIO1	IO	22	General Purpose Input/Output Pin
GPIO2	IO	23	General Purpose Input/Output Pin
GPIO3	IO	24	General Purpose Input/Output Pin

Symbol	Type	Pin No	Description
GPIO4	IO	46	General Purpose Input/Output Pin
GPIO5	IO	45	General Purpose Input/Output Pin
GPIO6	IO	20	General Purpose Input/Output Pin
GPIO7	IO	42	General Purpose Input/Output Pin
GPIO8	IO	44	General Purpose Input/Output Pin
GPIO9	IO	4	General Purpose Input/Output Pin
GPIO11	IO	43	General Purpose Input/Output Pin
GPIO12	IO	17	General Purpose Input/Output Pin
GPIO13	IO	18	General Purpose Input/Output Pin
GPIO14	IO	19	General Purpose Input/Output Pin
GPIO15	IO	47	General Purpose Input/Output Pin

6.10. Power Pins

Table 10. Power Pins

Symbol	Type	Pin No	Description
VD33D	P	37,38	3.3V for digital Circuit
VD33D	P	41	3.3V for digital Circuit and GPIO 7/8/9/11
SW_LX	P	36	Switching Regulator Output
VA33_PA_S0 VA33_PAD_S0 VA33_BT_SYN VA33_PAD_S1 VA33_PA_S1 VA33_WL_SYN VA33_AFE	P	1 2, 6 10, 12, 8, 14	3.3V for RF Analog Circuit
VDD_IO	P	28	VDD for GPIO 0 ~ GPIO6, GPIO10, GPIO12~GPIO15
VD1P25	P	40	VDD 1.25V Digital Circuit
VA1P25_RTX_S0 VA1P25_BT_SYN VA1P25_WL_SYN VA1P25_RTX_S1 VA1P25_AFE	P	3, 5 8 9 13	1.25V for RF analog circuit
SW_GND	P	35	Switching Regulator Ground

7. Electrical and Thermal Characteristics

7.1. Temperature Limit Ratings

Table 11. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

7.2. Power Supply DC Characteristics

Table 12. Power Supply DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VA33, VD33D	3.3V Supply Voltage	3.0	3.3	3.6	V
VDD_IO,	Digital IO Supply Voltage	1.62	1.8~3.3	3.6	V
VA1P25_RTX_S0 VA1P25_BT_SYN VA1P25_WL_SYN VA1P25_RTX_S1 VA1P25_AFE, VD1P25	1.25V Core Supply Voltage	1.15	1.25	1.37	V
IDD33	3.3V Rating Current	-	-	600	mA

7.3. Digital IO Pin DC Characteristics

Table 13. 3.3V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	-	0	0.9	V
V_{OH}	Output high voltage	2.97	-	3.3	V
V_{OL}	Output low voltage	0	-	0.33	V

Table 14. 2.8V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.8	2.8	3.1	V
V_{IL}	Input low voltage	-	0	0.8	V
V_{OH}	Output high voltage	2.5	-	3.1	V
V_{OL}	Output low voltage	0	-	0.28	V

Table 15. 1.8V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.3	1.8	2.0	V
V_{IL}	Input low voltage	-	0	0.8	V
V_{OH}	Output high voltage	1.62	-	1.8	V
V_{OL}	Output low voltage	0	-	0.18	V

7.4. SDIO/GSPI Interface AC Characteristics

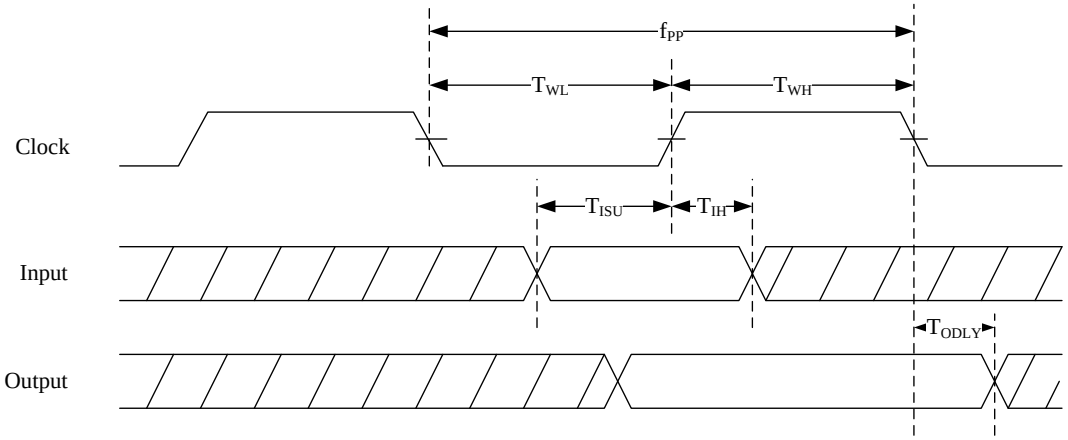


Figure 4. SDIO Interface Timing

Table 16. SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

7.4.1. SDIO/GSPI Interface Signal Levels

The SDIO and GSPI signal level ranges from 1.8V to 3.3V. The host provides the power source with the target power level to the RTL8723DS SDIO and GSPI interfaces via the VDIO_SDIO pin.

The 3.3V, 2.8V, and 1.8V DC characteristics of typical signal levels are shown in section 1.1 Digital IO Pin DC Characteristics, page 13.

7.4.2. SDIO Interface Power-On Sequence

After power-on, the SDIO interface is selected by the RTL8723DS automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended.

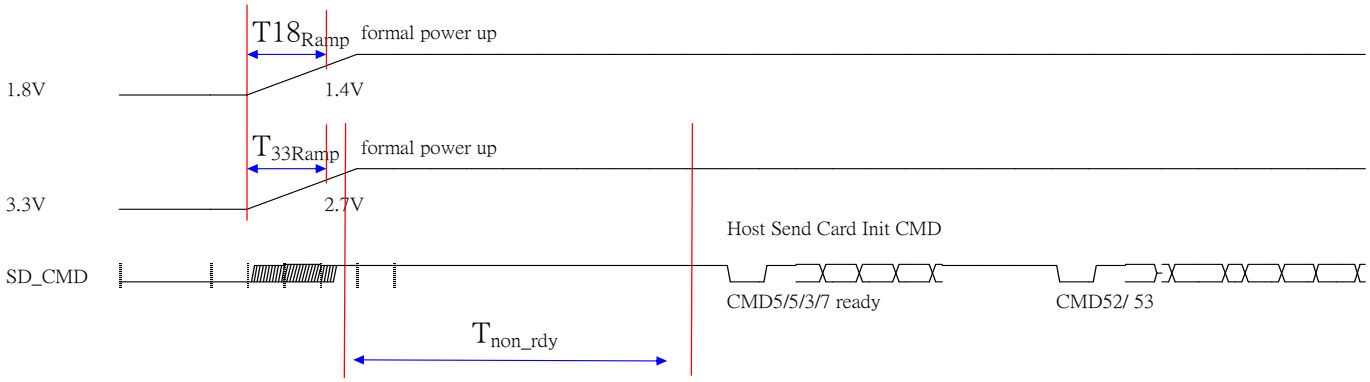


Figure 5. SDIO Interface Power-On Sequence

Table 17. SDIO Interface Power-On Sequence

Symbol	Description
T_{33ramp}	The 3.3V main power ramp up duration.
T_{18ramp}	The 1.8V main power ramp up duration.
T_{non_rdy}	SDIO Not Ready Duration. In this state, the RTL8723DS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

After main 3.3V ramp up and 1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SDIO block. eFUSE is then autoloaded to SDIO circuits during the T_{non_rdy} duration. After CMD5/5/3/7 procedures, card detection is executed. When the driver has loaded, normal CMD52 and CMD53 are used.

Table 18. SDIO Interface Power-On Timing Parameters

	Min	Typical	Max	Unit
T33ramp	0.2	0.5	2.5	ms
T18ramp	0.2	0.5	2.5	ms
Tnon-rdy	1	2	10	ms

7.4.3. GSPI Interface Power-On Sequence

The GSPI (Generic Serial Peripheral Interface) interface is enabled automatically when the first valid GSPI command is received.

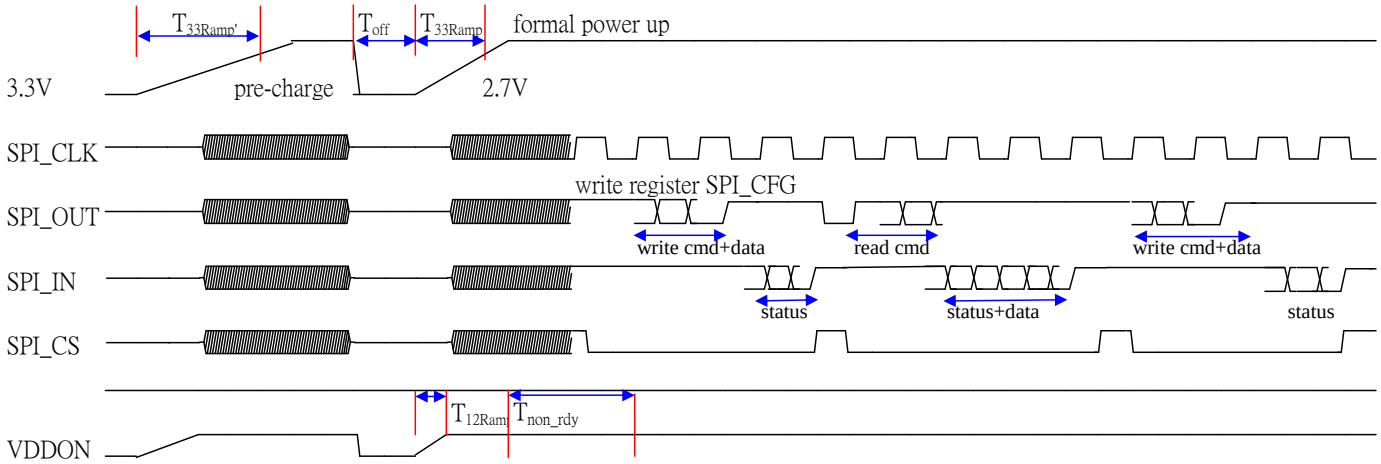


Figure 6. GSPI Interface Power-On Sequence

Table 19. GSPI Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on sequence and then a following power-off sequence is executed by the host controller before the formal power on sequence. This procedure can avoid host card detection failure issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration from 3.3V cut off time to the beginning of next formal power up.
T_{33ramp}	The 3.3V main power ramp-up duration.
T_{12ramp}	The internal 1.2V ramp-up duration.
T_{non_rdy}	SPI Not Ready Duration. After T_{non_rdy}, SPI host can then send commands to write SPI_CFG register. SPI_CFG register is used for SPI endian and word length control.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SPI block. eFUSE is then autoloaded to SPI circuits during the T_{non_rdy} duration.

Table 20. SPI Interface Power-On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}	0.2	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
$T_{non\text{-}rdy}$	3	4	18	ms

7.5. UART Interface Characteristics

The RTL8723DS UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2k baud. In order to support high and low speed baud rate, the RTL8723DS provides multiple UART clocks.

Table 21. UART Interface Power-On Timing Parameters

Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%
600	600	0.00%
900	900	0.00%
1200	1200	0.00%
1800	1800	0.00%
2400	2400	0.00%
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%
128000	127119	-0.69%
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

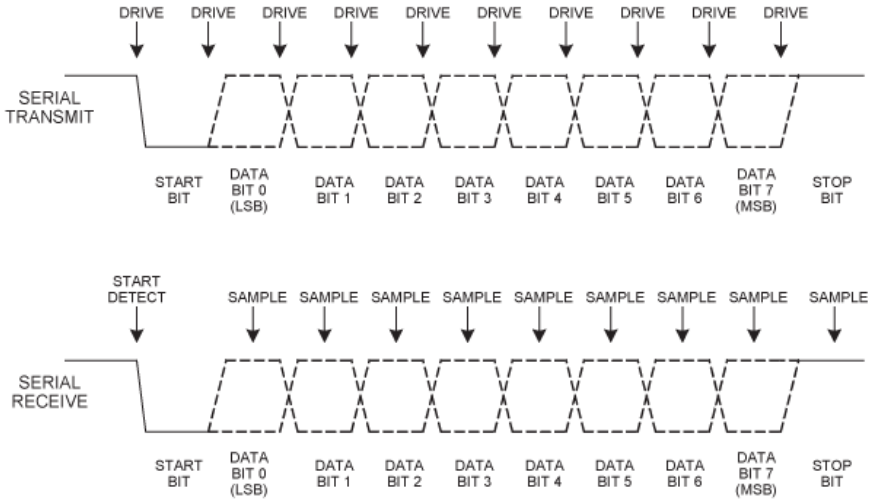


Figure 7. UART Interface Waveform

7.5.1. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8723DS UART interface via the VDIO_SDIO pin.

The 3.3V, 2.8V, and 1.8V DC characteristics of typical signal levels are shown in section 1.1 Digital IO Pin DC Characteristics, page 13.

7.5.2. UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

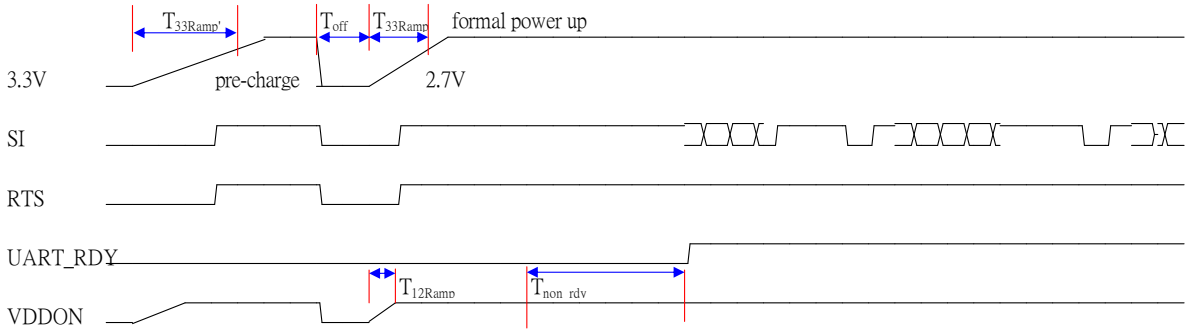


Figure 8. UART Power-On Sequence With Hardware Flow Control

UART Hardware Flow Control Supported

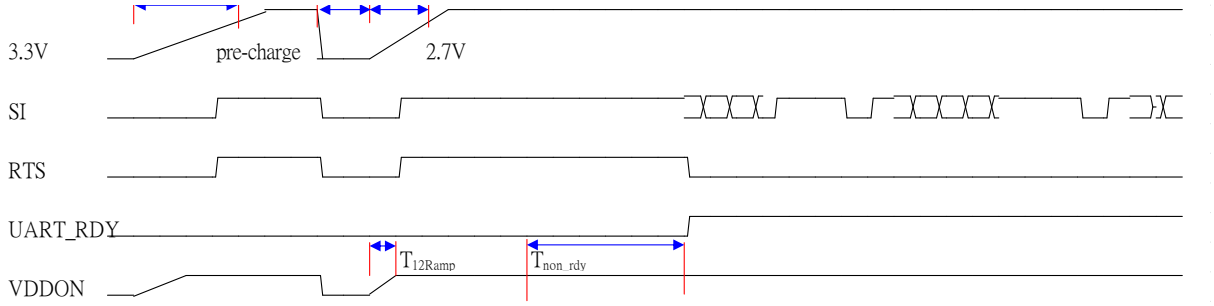


Figure 9. UART Power-On Sequence Without Hardware Flow Control

Table 22. UART Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8723DS will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits, included the UART. In addition to wait the T_{non_rdy} time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

Table 23. UART Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}	0.2	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms

	Min	Typical	Max	Unit
$T_{non-rdy}$	1	2	10	ms

7.6. PCM Interface Characteristics

The RTL8723 supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

7.6.1. PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (错误!未找到引用源。), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (错误!未找到引用源。).

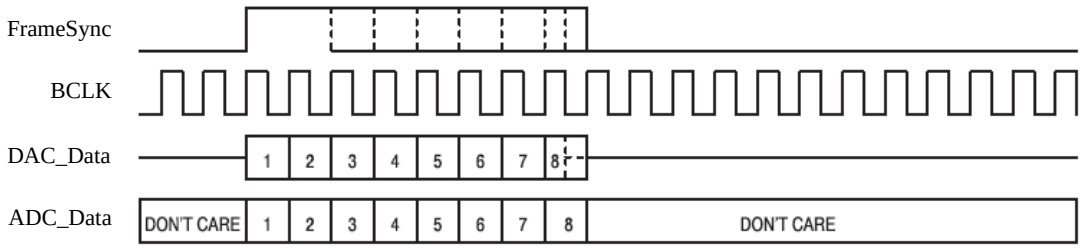


Figure 10. Long FrameSync

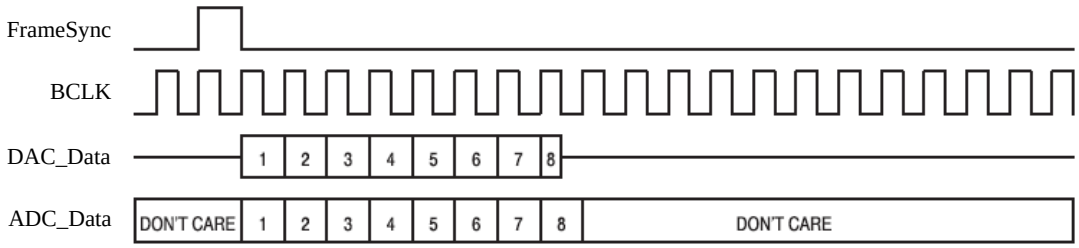


Figure 11. Short FrameSync

7.6.2. Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

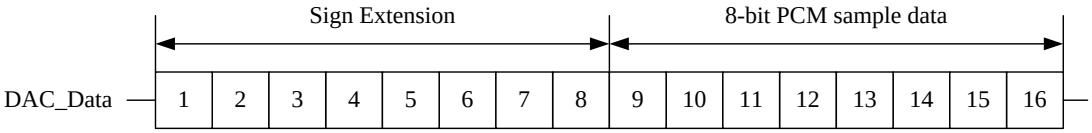


Figure 12. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

Figure 13. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

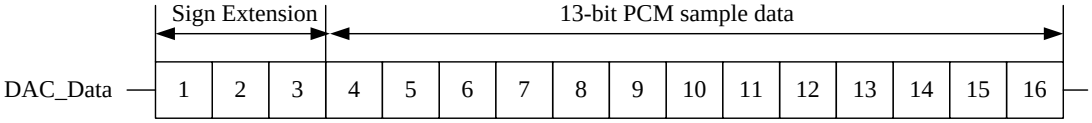


Figure 14. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

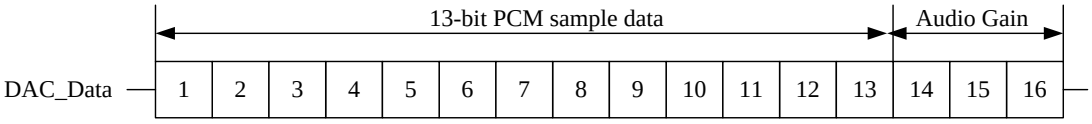


Figure 15. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

7.6.3. PCM Interface Timing

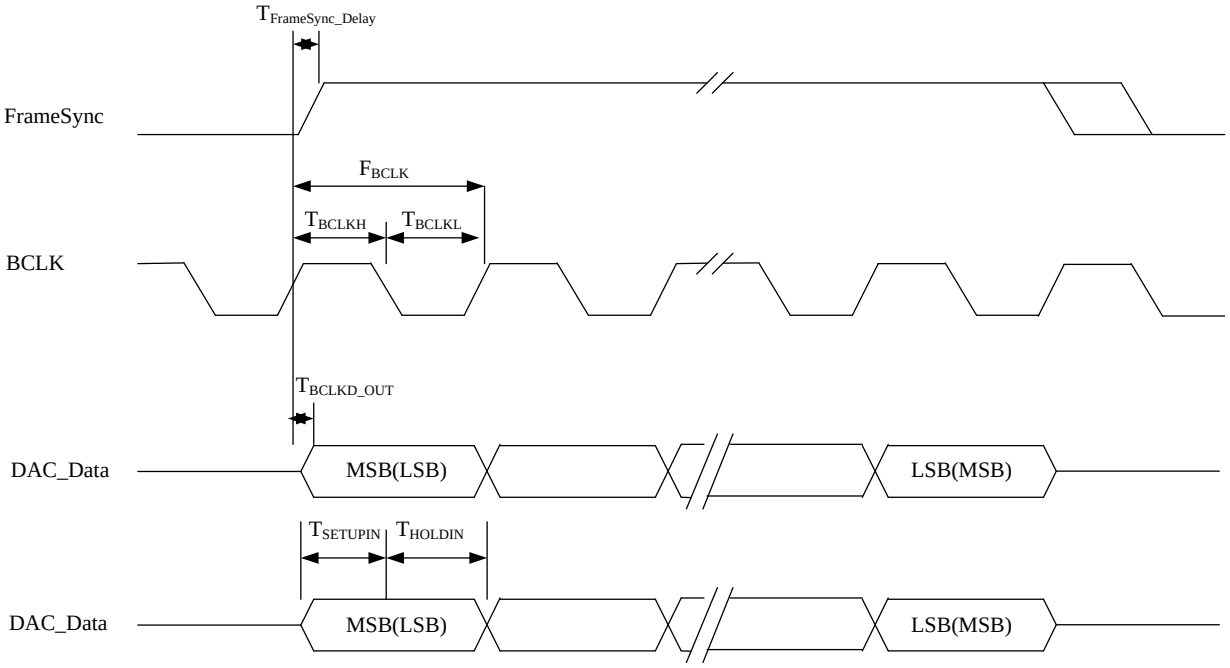


Figure 16. PCM Interface (Long FrameSync)

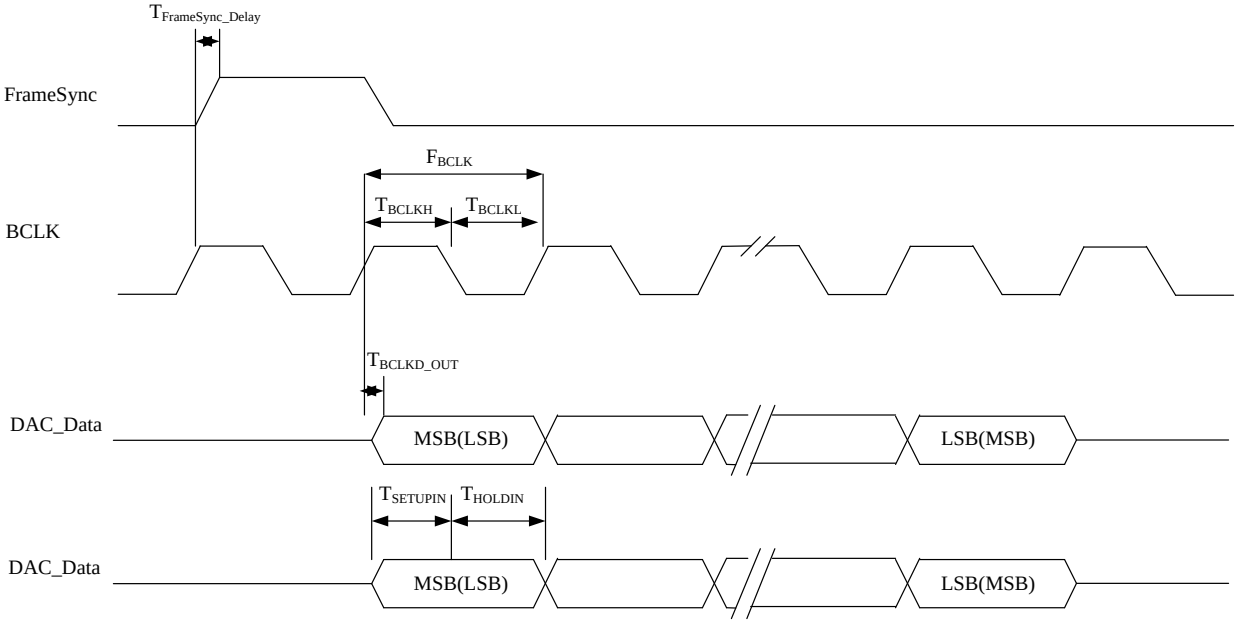


Figure 17. PCM Interface (Short FrameSync)

Table 24. PCM Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	-	kHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	kHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 25. PCM Interface Timing

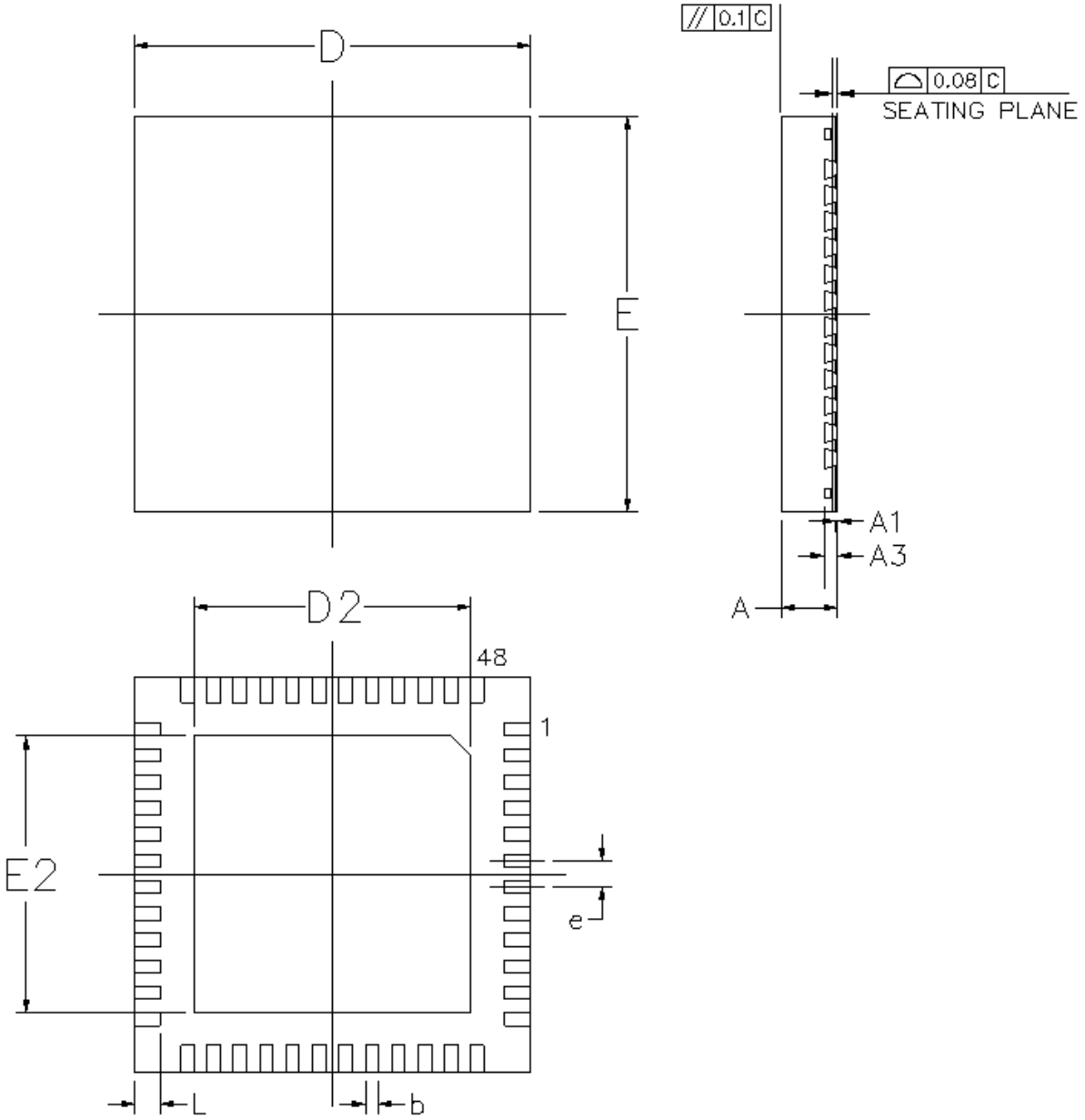
Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$T_{FrameSync\_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns
T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

7.6.4. PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8723DS PCM interface via the VDD_IO pin .

The 3.3V, 2.8V, and 1.8V DC characteristics of typical signal levels are shown in section 1.1 Digital IO Pin DC Characteristics, page 13.

8. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		

D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note1: CONTROLLING DIMENSION：MILLIMETER(mm)

Note2: REFERENCE DOCUMENTL：JEDEC MO-220

9. Ordering Information

Table 26. Ordering Information

Part Number	Package	Status
RTL8723DS-CG	QFN-48, 'Green' Package	Engineering Samples

Note: See page 7 for package identification.

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